What is claimed is:

1. A discontinuous transmission (DTX) bit processing method for a multirate modulation scheme comprising:

receiving a symbol;

determining whether the symbol comprises at least one DTX bit;

mapping the symbol to a predetermined mapping point (S) on an IQ plane;

minimizing a transmission power level if the symbol has at least one DTX bit; and

transmitting the symbol in the transmission power level of the mapping point.

2. The method of claim 1, wherein the mapping point is calculated by averaging signal points in which bits corresponding to non-DTX bits of the symbol are approximately identical with each other on the IQ plane.

3. The method of claim 2, wherein the mapping point is set in consideration of at least one of a number of the non-DTX bits, a number of the selected signal points, and locations of the selected signal points on the IQ plane.

4. The method of claim 1, wherein the symbol is mapped to an origin of the IQ plane, when at least one bit of the symbol is a DTX bit.

5. The method of claim 1, wherein the symbol is mapped to a signal point in which bits are identical with the bits consisting of the symbol on the IQ plane, when the symbol has no DTX bits.

6. The method of claim 2, wherein the mapping point is set in consideration of plus and minus symbols of the signal points on the IQ plane.

7. The method of claim 6, wherein the mapping point is set in consideration of at least one of number of the non-DTX bits, number of the selected signal points, and locations of the selected signal points on the IQ plane.

8. The method of claim 7, wherein the symbol is mapped to an origin of the IQ Plane, when at least one bit of the symbol is a DTX bit.

9. The method of claim 8, wherein the symbol is mapped to a signal point in which bits are approximately identical with bits comprising the symbol in the IQ plane, if the symbol has no DTX bit.

10. A transmitter of a base station modem comprising:

a transport channel (TrCH) multiplexer for multiplexing radio frames from a plurality of transport channels into a composite transport channel (CCTrCH);

a discontinuous transmission (DTX) insertion module for inserting DTX bits into the radio frames of the CCTrCH;

a physical channel segmentation module for segmenting the CCTrCH for different physical channels (PhCHs) to produce a plurality of segments;

an interleaver for interleaving the segments; and

a physical channel mapping module for mapping the segments to the corresponding PhCHs.

11. A discontinuous transmission (DTX) bit processing system

comprising:

means for receiving a symbol;

means for determining whether the symbol comprises at least one DTX bit;

means for mapping the symbol to a predetermined mapping point (S) on an IQ plane;

means for minimizing a transmission power level if the symbol has at least one DTX bit; and

means for transmitting the symbol in the transmission power level of the mapping point.

12. The system of claim 11, wherein the mapping point is calculated by averaging signal points in which bits corresponding to non-DTX bits of the symbol are approximately identical with each other on the IQ plane.

13. The system of claim 12, wherein the mapping point is set in consideration of at least one of a number of the non-DTX bits, a number of the selected signal points, and locations of the selected signal points on the IQ plane.

14. The system of claim 11, wherein the symbol is mapped to an origin of the IQ plane, when at least one bit of the symbol is a DTX bit.

15. The system of claim 11, wherein the symbol is mapped to a signal point in which bits are identical with the bits consisting of the symbol on the IQ plane, when the symbol has no DTX bits.

16. The system of claim 12, wherein the mapping point is set in

consideration of plus and minus symbols of the signal points on the IQ plane.

17. The system of claim 16, wherein the mapping point is set in consideration of at least one of number of the non-DTX bits, number of the selected signal points, and locations of the selected signal points on the IQ plane.

18. The system of claim 17, wherein the symbol is mapped to an origin of the IQ Plane, when at least one bit of the symbol is a DTX bit.

19. The system of claim 18, wherein the symbol is mapped to a signal point in which bits are approximately identical with bits comprising the symbol in the IQ plane, if the symbol has no DTX bit.